REMARKS

The Applicants respectfully request further examination and reconsideration in view of the above preliminary amendment. By this preliminary amendment applicants have amended claims 6, 7 and 14. Accordingly, after the above preliminary amendment claims 1-21 are now pending.

Applicants respectfully submit that the claims, as amended, are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (408) 530-9700 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: 6-14-02

By: _____
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CERTIFICATE OF MAILING (37 CFR § 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington D.C. 20231

HAVERSTOCK & OWENS LLP

Date: _____ By: _____

Version with markings to show changes made.

IN THE CLAIMS:

6. (Amended) A mixer circuit for generating an IF output responsive to an RF input and a LO drive source, comprising:

a mixer core having a doubly balanced mixer including a first differentially coupled npn transistor pair and a second differentially coupled npn transistor pair, the mixer core coupled to receive a LO drive signal, the LO drive signal having a plurality of harmonics;

a low noise RF input circuit coupled to the mixer core through a folded cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the folded cascode circuit further isolates the RF input circuit from the LO drive signal and the plurality of harmonics.

7. (Amended) A mixer as in Claim 6 wherein the folded cascode circuit comprises:

a first cascode transistor having an emitter terminal coupled to [the]a second terminal of [the]a first capacitor and to [the]a first terminal of [the]a third inductor, a collector terminal coupled to the second differentially coupled npn transistor pair and a base terminal,

a second cascode transistor having a base terminal coupled to the base terminal of the first cascode transistor, an emitter terminal coupled to [the]a first terminal of [the]a second inductor and to [the]an emitter terminal of [the]a first npn transistor and a collector terminal coupled to the first differentially coupled npn transistor pair,

a second capacitor, having a first terminal coupled to the [collector]emitter terminal of the [first]second cascode transistor and a second terminal coupled to a second terminal of the first capacitor, the base terminal of the first cascode transistor and to the base terminal of the second cascode transistor,

a third capacitor, having a first terminal coupled to the emitter terminal of the [second]first cascode transistor and a second terminal coupled to the second terminal of the second capacitor[and to the base terminal of the first cascode transistor and to the base terminal of the first cascode transistor],

a second biasing resistor having a first terminal coupled to the [second]first terminal of the [third]second capacitor and a second terminal coupled to a second bias voltage.

14. (Amended) A quadrature mixer circuit for generating a quadrature IF output responsive to an RF input and a quadrature pair of LO drive signals, comprising:

a mixer core having a first doubly balanced mixer including a first differentially coupled npn transistor pair and a second differentially coupled npn transistor pair and having a second doubly balanced mixer including a third differentially coupled npn transistor pair and a fourth differentially coupled npn transistor pair; the mixer core coupled to receive a quadrature LO drive signal, the quadrature LO drive signal having a plurality of harmonics;

a low noise RF input circuit coupled to the mixer core through a folded cascode circuit, the low noise RF input circuit coupled to receive an RF input signal, wherein the folded cascode circuit further isolates the RF input circuit from the quadrature LO drive signal and the plurality of harmonics,

a first cascode capacitor, a first terminal of the first cascode capacitor coupled to the emitter terminal of a first cascode transistor and a second node of the first cascode capacitor coupled to the base terminals of the first cascode transistor and a second cascode transistor,

a second cascode capacitor, a first terminal of the second cascode capacitor coupled to the base terminals of the first cascode transistor and the second cascode transistor and the second node of the second cascode capacitor coupled to the emitter terminal of the second cascode transistor.